Introduction

Many of the techniques used for the modelling of PCB track make use of the SPICE transmission line. There are distinct disadvantages to this approach, chief of which is the fact that model parameters are difficult to derive from real-world measurements, and the behaviour of the final model is rarely representative of the actual circuit. Additionally, complex circuits may lead to convergence problems.

We present an implementation of the scaleable modelling approach, outlined in the paper by Ladd & Costache, which is easily related to measurable circuit board parameters, and whose components we have included in the library “pcb”.

One enhancement that we have made to the original design, is an alternative model of the plated-through hole, or via, whose parameters may be readily derived from physical data.

The test circuits shown later will enable predictions to be made of the crosstalk between adjacent PCB tracks. There are two sets of tests available, one set on a three track topology, with a ground conductor between the two tracks being tested, and one on a two-track topology, where there is no ground conductor.

Running these tests, using the original topology and component values gave results which differed slightly from those shown in the original paper, so we conclude that the differences reflect the different versions of the SPICE simulator used.

The crosstalk effects modelled here, include electrostatic and electromagnetic coupling between the tracks. Also, since the current in each segment can be measured, the current distribution along the line can be simulated. This means that the electric field emanating from the track can also be estimated, at various distances from the board.

The Basic Element

The transmission lines formed by any PCB track can be broken up into electrically short segments, such that the segment length is less than or equal to one-tenth of the wavelength of interest.

For the maximum bandwidth of 1.3GHz, to be considered in the example below, which concerns itself with a track length of 10cm, we would need an element length of less than one tenth of a wavelength of 1.3GHz, i.e

\[ \text{Element length} < \frac{1}{10} \times \left( \frac{3 \times 10^10}{1.3 \times 10^9} \right) = 2.3\text{cm} \]

We, therefore, determine our minimum track element to be a 2cm length, which is represented by the lumped equivalent circuit, shown in Figure 1.
Note that the basic element actually comprises two 1 cm segments, to represent the 2 cm element.

**Figure 1**

Two Parallel Track Segments

Figure 2 shows the complete base element used to model a 2 cm section of two parallel tracks.

**Figure 2**
The crosstalk is generated by way of capacitive coupling, and by way of coupling between the inductors of the upper track (T1A - T1B), and those of the parallel track (T2A – T2B).

In that context, it should be noted that the inductors have extra properties. Each inductor has a COUPLED property, which references the LOCATION property of the corresponding inductor in the parallel track, into which the crosstalk is to be injected.

If we were designing an actual transformer, the PARAMS parameter would contain the number of turns on the winding, from which the netlist compiler would calculate the coupling coefficient as per:

$$K_{12} = \frac{N_2}{N_1} \times \sqrt{\frac{L_1}{L_2}}$$

In this case, however, we already know the coupling coefficient, having calculated it in Appendix 1, so it would be convenient to enter it on the drawing, rather than edit the netlist.

It may be seen that, in the circuit shown in Figure 2, the pairs of coupled inductors have identical values, so the equation above reduces to

$$K_{12} = \frac{N_2}{N_1}$$

So we can set the PARAMS value directly to the coupling coefficients, and they pass unaltered through the netlist compiler.

**Two Tracks with GROUND Conductor**

Figure 3 includes a third, GROUND, conductor midway between the transmitting track and the receiving track.

Now, the coupling coefficients cannot simply be entered directly.
As may be seen from Appendix 1, we will need a coupling coefficient of 0.1099 from tracks (T1A – T1B) and (T2A – T2B) to the ground track (T3A – T3B).

Because the tracks have different widths, the track inductance is 1.8185nH, while the ground inductance is 2.026nH.

We set the track with the lower value to a ‘turns’ value of ‘1’ and calculate ‘turns’ for the higher value:

\[
L_1 = 2.026 \times 10^{-9} \\
L_2 = 1.8185 \times 10^{-9} \\
K = 0.1099
\]

\[
\frac{N_2}{N_1} = \frac{K}{\sqrt{L_1/L_2}}
\]

We set N2 to 1, so

\[
\frac{1}{N_1} = \frac{0.1099}{\sqrt{2.026 \times 10^{-9} / 1.8185 \times 10^{-9}}}
\]

\[
N_1 = \sqrt{\frac{2.026 \times 10^{-9}}{1.8185 \times 10^{-9}}} / 0.1099
\]

\[
= \sqrt{1.1141} / 0.1099
\]

\[
= 9.6043
\]

Running the drawing through the netlist compiler results in the netlist of Appendix 2, which contains the correct coupling coefficients.

**The Via**

A via or, plated-through hole, connects tracks between PCB layers. For reasonably high bandwidth boards, such as the 1.3GHz example we are considering, a via represents a discontinuity in the signal flow, having an effective impedance of approximately 60 ohms.

For the test circuits discussed in this paper, we will assume a non-HDI, single layer, double-sided board, of height 1.588mm (0.625 inch), containing vias of diameter 0.2mm (0.0676 inch), with a pad diameter of 0.3mm. Further, we can assume the plating thickness to be 0.0254 mm.

Since opinions among researchers differ on whether a via is totally capacitive, or totally inductive, we take the approach that it is, in fact, both, and provide non-rigorous methods of calculating the inductance and capacitance from the physical dimensions and materials.

Additionally, we take into account the ohmic resistance of the through-plating, across which both the inductive and capacitive currents flow.

**Via Inductance**

\[
L = 12.57 \times 10^{-7} \times \frac{h}{2\pi} \times (\ln(4 \times h / d) + 1)
\]

Where \( d \) = via diameter and \( h \) = PCB thickness (barrel length)

\[
L = (12.57 \times 10^{-7} \times (1.588 \times 10^{-3})) / 6.2832 \times (\ln(4 \times 1.588 \times 10^{-3} / 0.2 \times 10^{-3}) + 1)
\]

\[
= (1.9961 \times 10^{-9} / 6.2832) \times (\ln(4 \times 7.94) + 1)
\]

\[
= 3.1769 \times 10^{-10} \times (3.4582 + 1)
\]

\[
= 1.4163 \text{nH}
\]
**Via capacitance**

\[ C_{via} = 2\pi \cdot e \cdot \varepsilon_0 \cdot \frac{h}{\ln(rp / r)} \]

Where \( r \) = via radius, \( rp \) = pad radius and \( h \) = PCB thickness (barrel length)

\[
C = 2\pi \cdot (4.7 \cdot 8.85\times10^{-12}) \cdot 1.588\times10^{-3} / \ln(0.15\times10^{-3} / 0.1\times10^{-3}) \\
= 4.1502\times10^{-13} / \ln(1.5) \\
= 4.1502\times10^{-13} / 0.40546 \\
= 1.02356\times10^{-12} = 1.0235pF
\]

This will resonate with the inductance at a frequency

\[
f = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \\
= 1 / (6.2832 \cdot \sqrt{1.4163\times10^{-9} \cdot 1.02356\times10^{-12}}) \\
= 1 / (6.2832 \cdot 3.8075\times10^{-11}) \\
= 1 / 2.9232e-10 \\
= 4.18e9 = 4.18\text{gHz}
\]

**Via Resistance**

Any crosstalk current will flow radially from the inside to the outside of the via, so we calculate the DC resistance of a cylinder driven in such a manner from

\[
R = \frac{\rho}{2\pi \cdot h} \cdot \ln(r_2 / r_1)
\]

Where \( \rho \) = via resistivity, \( h \) = via length, \( r_1 \) = inner radius, and \( r_2 \) = outer radius.

Given that the via’s outer radius is 0.1mm and the plating thickness is 0.0254\times10^{-3}, its inner radius will be 0.0746mm

For a copper via, the resistivity, \( \rho \), is 0.000002 = 2e-6 ohm-cm, so the resistance of the via is

\[
R = \frac{(2e-6 \cdot (6.28 \cdot 1.588\times10^{-3})) \cdot \ln(0.10\times10^{-3} / 0.0746\times10^{-3})}{(2e-6 \cdot 9.9777\times10^{-3}) \cdot \ln(1.34)} \\
= 2.0045e-4 \cdot 0.29303 \\
= 58.7378e-6 \text{ohms.}
\]

Figure 4 shows the equivalent circuit of a plated through hole, using the values calculated above.

Figure 5 is the schematic symbol we have created for it.
The via will be used for grounding the central conductor in our 10cm test circuit, which is made up of five 2cm elements. Each via will, obviously, be 2cm from its neighbour (1/10th the wavelength at 1.3GHz) for optimum crosstalk suppression.
The Test Circuits

The examples, 'ten_seg' and 'ten_cm' both represent a 10cm section of parallel track, made up of five 2cm segments. They differ in that 'ten_seg' is a two-track test circuit, while 'ten_cm' is a three-track circuit. Both models are to be found in the 'pcb; library.

Two 10cm Parallel Tracks With No Ground

We create a circuit symbol to represent the schematic of Figure 2 as shown below, in Figure 6.

![Figure 6](image)

We then add 5 instances of the symbol to create the test schematic of Figure 7.

The top line is driven with a voltage source defined by the line

```
pwl 0 0 1n 0 6n 1 40n 1 46n 0 80n 0 AC 1
```

Which signifies a pulse, which starts a zero volts, rises to 1volt between 1ns and 6ns, then stays at 1volt till 40ns, then drops to zero at 46ns, where it remains till 80ns. The ‘AC 1’ parameter is a nominal value, only used for the frequency domain analysis.

The lower line is terminated at its near end in 33 ohms, while the far ends of both lines drive a 100 ohm load resistor.
Two 10cm Parallel Tracks Separated by a Central Ground Conductor

We create a circuit symbol to represent the schematic of Figure 3 as shown below, in Figure 8.
The schematic is created as shown below, using our ‘two_cm’ component, and the via, created earlier. It may be seen that we connect the central ground line, through a via, to true ground every 2cm.
As before, the driving source is defined as

```
pwl 0 0 1n 0 6n 1 40n 1 46n 0 80n 0 AC 1
```

Both lines drive 100 ohm load resistors, and the lower line is, again, terminated with 33 ohms at its near end.

![Figure 9](image-url)
Simulation

Two Conductors with Ground Track

AC Analysis
The following SPICE command sets a resolution of 2000 points per decade, which gives a clean, smooth set of curves, and we sweep the frequency from 1 MHz to 1.3 GHz.

.ac dec 2000 1meg 1.3g

Although the waveforms at the junctions of all segments are available, in the interests of clarity, we limit the plot to VT2A and VOUT, i.e those at the near and far ends of the receiving track, T2. The response curves are best viewed on a linear Y-scale, rather than dB, to emphasise the points of inflection.

The response shows a rising characteristic, with two points of inflection. For the near-end response (VT2A), the first is situated at approximately 600 MHz, while the second occurs at 930 MHz.

The far-end curve (VT25) rises more steeply, the first inflection point being at around 420 MHz, and the second at around 800 MHz.
Transient Analysis

The time-domain measurements are made on both ends of the receiving track. The analysis is set up to plot 0 to 100ns in 10ps steps.

.tran 10p 100n 0

It will also be necessary to set .options method=gear to remove the spurious oscillations that SPICE is known to produce when simulating RLC circuits.

The transmitting track is driven by a rectangular pulse, defined by

pwl 0 0 1n 0 6n 1 40n 1 46n 0 80n 0 AC 1

The circuit simulation produces the result shown below, which is worthy of a short discussion.
This is a transmission line, with a total delay of 5ns, so the delay between each segment is 1ns. The leading edge of the driving waveform travels down the transmission line, and so do the crosstalk pulses. As each pulse arrives at the segment junction

![Figure 11](image.png)

The results show two pulses in the near-end waveform (VT2A), both 5ns wide, coincident with the rising and falling edges. The magnitudes are about 400-800uV for the positive pulse, and about 500-650uV for the negative one.

The near end (VT2A) and far end (VT25) outputs are probably the most interesting, and are shown below, in Figure 12, for closer inspection.
AC Analysis

We will need to plot the frequency characteristics of each circuit, to check the accuracy of our predictions. A resolution of **2000 points per decade** gives a clean, smooth set of curves, and we sweep the frequency from **1 MHz to 1.3 GHz**.

\[ .ac \text{ dec 2000 1meg 1.3g} \]
Although the frequency response shows the same inflection points as for the three-track model, the transient analysis for two-track topology shows more crosstalk, as may be seen from Figures 14 and 15, below.
Three Tracks Two Ground Vias

A special drawing, '10cm2via' simulates the case where the ground conductor is only provided with a via at each end.

Figure 16

An analysis of this circuit shows a large resonance peak at around 800MHz, this being the frequency for which 10cm is a quarter wavelength.

Figure 17
We can confirm the frequency, as follows:

Taking the propagation velocity as $3.16 \times 10^{10}$ cm/sec:

$$3.16 \times 10^{10} = f \times 40$$

$$f = 790 \text{ MHz}$$

The pole-zero plot is as below:

![Figure 18](image)

The transient analysis is performed using the same stimulus waveform as used for the multiple via circuit. The result shows an increase in the amount of crosstalk.

![Figure 19](image)
Appendix 1

All tracks are **2.5mm** wide, and have (width / height) set at **1.58** such that the characteristic impedance is **58 ohms**. The tracks are set **7.5mm** apart, from inside edge to inside edge, on a glass epoxy PCB, with a dielectric constant of **4.7**.

The circuit values have been calculated from distributed parameter data, obtainable either from the PCB manufacturer, or from finite-element analysis.

The lumped model parameters for the PCB tracks are derived from the distributed parameters by multiplying by the line length and dividing by the number of segments.

The per-unit-length parameters for tracks of the above dimensions and spacing are as follows:

<table>
<thead>
<tr>
<th>Component</th>
<th>2 track</th>
<th>3 track</th>
</tr>
</thead>
<tbody>
<tr>
<td>C10</td>
<td>95.3 pF/m</td>
<td>91.9 pF/m</td>
</tr>
<tr>
<td>C12</td>
<td>0.459 pF/m</td>
<td>0.185 pF/m</td>
</tr>
<tr>
<td>C13</td>
<td>-</td>
<td>4.30 pF/m</td>
</tr>
<tr>
<td>C20</td>
<td>95.3 pF/m</td>
<td>91.9 pF/m</td>
</tr>
<tr>
<td>C23</td>
<td>-</td>
<td>4.30 pF/m</td>
</tr>
<tr>
<td>C30</td>
<td>-</td>
<td>79.5 pF/m</td>
</tr>
<tr>
<td>L11</td>
<td>374.2 nH/m</td>
<td>363.7 nH/m</td>
</tr>
<tr>
<td>L12</td>
<td>13.22 nH/m</td>
<td>12.90 nH/m</td>
</tr>
<tr>
<td>L13</td>
<td>-</td>
<td>42.20 nH/m</td>
</tr>
<tr>
<td>L22</td>
<td>374.2 nH/m</td>
<td>363.7 nH/m</td>
</tr>
<tr>
<td>L23</td>
<td>-</td>
<td>42.20 nH/m</td>
</tr>
<tr>
<td>L33</td>
<td>-</td>
<td>405.2 nH/m</td>
</tr>
</tbody>
</table>

**Parameters For Three Track Topology**

- From the above, the value of inductors L1, in 1cm of transmitting line:

  \[ L1 = \frac{(L11 / 100)}{2} = \frac{(3.637 / 2)}{\text{nH}} \] (as there are 2 per cm)

  \[ = 1.8185 \text{nH} \]

- For all inductors L2, in 1cm of receiving line:

  \[ L2 = \frac{(L22 / 100)}{2} = \frac{(3.637 / 2)}{\text{nH}} \] (as there are 2 per cm)

  \[ = 1.8185 \text{nH} \]

- For all inductors L3, in 1cm of ground line

  \[ L3 = \frac{(L33 / 100)}{2} = \frac{(4.052 / 2)}{\text{nH}} \]

  \[ = 2.026 \text{nH} \]

- The inductive coupling coefficients, from each line to the ground conductor, are given by:
\[ K_{ab} = \frac{L_{ab}}{\sqrt{L_a \times L_b}} \]

Thus,

\[
K_{13} = \frac{L_{13}}{\sqrt{L_{11} \times L_{33}}} \\
= \frac{42.2 \times 10^{-9}}{\sqrt{363.7 \times 10^{-9} \times 405.2 \times 10^{-9}}} \\
= 0.109927
\]

\[
K_{23} = \frac{L_{23}}{\sqrt{L_{22} \times L_{33}}} \\
= \frac{42.2 \times 10^{-9}}{\sqrt{363.7 \times 10^{-9} \times 405.2 \times 10^{-9}}} \\
= 0.109927
\]

Note: SPICE transformers are bi-directional, but we only need to calculate one coupling coefficient.

Since there is only one capacitor per 1cm segment, the capacitor values are:

\[
C_{1} = C_{10} / 100 = 0.919 \text{pF} \\
C_{12} = C_{12} / 100 = 0.00185 \text{pF} \\
C_{13} = C_{13} / 100 = 0.043 \text{pF} \\
C_{2} = C_{20} / 100 = 0.919 \text{pF} \\
C_{23} = C_{23} / 100 = 0.043 \text{pF} \\
C_{3} = C_{30} / 100 = 0.795 \text{pF}
\]

**Parameters for Two Track Topology (No Ground Line)**

With just two tracks, the values all need to be recalculated from the figures in the first column:

\[
L_{1} = \frac{(L_{11} / 100)}{2} = \frac{374.2}{200} \text{nH} = 1.871 \text{ nH} \\
L_{2} = \frac{(L_{22} / 100)}{2} = \frac{374.2}{200} \text{nH} = 1.871 \text{ nH}
\]

The only inductive coupling is now from \( L_1 \rightarrow L_2 \), so

\[
K_{12} = \frac{L_{12}}{\sqrt{L_{11} \times L_{22}}} \\
= \frac{13.22 \times 10^{-9}}{\sqrt{374.2 \times 10^{-9} \times 374.2 \times 10^{-9}}} \\
= 0.0353287
\]

The new capacitances are:

\[
C_{1} = C_{10} / 100 = 0.953 \text{pF} \\
C_{12} = C_{12} / 100 = 0.00459 \text{pF} \\
C_{2} = C_{20} / 100 = 0.953 \text{pF}
\]
Appendix 2

Via Considerations

The equations we use for calculating the via inductance and capacitance assume that:
1. The via stub has been back-drilled, to avoid creating a resonator.
2. The via pads are circular
3. The distance between the via outer edge and the via pad inner edge is small, and comparable to the distance from the via to the PCB’s reference planes.

Via plating thickness is generally half of the board copper thickness. If the hole size is 0.2mm, the diameter is 0.3mm and the board is plated with 35um copper, then the result will be as follows:
- a copper pad with a diameter of 0.3mm
- inside which is a plated hole where the plating has a thickness of 0.035mm
- The finished hole has a diameter of 0.13mm (0.2mm - 0.035mm*2).

The via parameters affect impedance as follows:
- **Hole diameter:** higher diameter = lower inductance, lower impedance
- **Pad diameter:** higher diameter = higher capacitance, lower impedance
- **Spacing between via and the hole in the ground plane:** higher spacing = lower capacitance, higher impedance
- **Board thickness:** higher thickness = higher inductance for the via and lower capacitance for the pads so, higher impedance

### Via impedance:
\[ \text{via}_Z0 = \sqrt{\text{via}_L / (\text{via}_C * 0.001)} \]

### Via Inductance:
\[ \text{Via}_L = 12.57e^{-7} \times h / 2\pi \times (\ln(4 \times h / d) + 1) \]

### Via Capacitance:
\[ \text{Via}_C = 2\pi \times er \times e0 \times (h / \ln(rp / r)) \]

Where:
- \( h \) = via length
- \( rp \) = pad radius
- \( r \) = via radius.
- \( d \) = via diameter
- \( er \) = relative permittivity or dielectric constant (~4.7)
- \( e0 \) = absolute permittivity or dielectric constant (8.85e-12)

\( (er = es / e0 \) where \( es \) is in F/m and \( e0 \) is in F/m so, \( es = er \times e0 \) \)
Quick’n’Dirty Via Ohmic Resistance

Surface area of via outer layer = \(2\pi \times r \times h = 2\pi \times 0.1 \times 3.14159 \times 1.588 \times 10^{-3} = 9.9777 \times 10^{-7}\)

Thickness of plating is \(0.035 \times 10^{-3} = 35 \times 10^{-6}\)

Resistance = \(\rho \times h \times \text{Area} = 2 \times 10^{-6} \times 0.035 \times 10^{-3} / 9.9777 \times 10^{-7} = 70 \times 10^{-6} \text{ ohms}\)
Appendix 3

Netlist of 2cm segment

2cm
.tran
.print
*iplot all
*#run
*#quit
K0 L11 L33A 0.109903
K1 L12A L33B1 0.109903
K2 L12B L33B2 0.109903
K3 L13 L33C 0.109903
K4 L21 L33A 0.109903
K5 L22A L33B1 0.109903
K6 L22B L33B2 0.109903
K7 L23 L33C 0.109903

L11 6 1  1.8185N
C1 1 0  0.919P
C2 3 0  0.919P
C3 1 13  0.00185P
C4 1 7  0.043P
C5 3 9  0.043P
C6 3 15  0.00185P
L12A 1 2  1.8185N
L12B 2 3  1.8185N
L13 3 4  1.8185N
L33A 11 7  2.026N
L33B1 7 8  2.026N
L33B2 8 9  2.026N
L33C 9 10  2.026N
L21 17 13  1.8185N
L22A 13 14  1.8185N
L22B 14 15  1.8185N
L23 15 16  1.8185N
C7 15 0  0.919P
C8 13 0  0.919P
C9 7 13  0.043P
C10 9 15  0.043P
C11 7 0  0.795P
C12 9 0  0.795P
.end